IN THE CLAIMS

Please amend the claims as follows:

Claim 1-26 (Canceled).

Claim 27 (Currently Amended): A semiconductor device comprising:

a supporting substrate including a first region and a second region, a surface of the [[first]] second region having a position lower than a position of a surface of the ~~second~~ first region;

a buried oxide layer formed on the first region of the supporting substrate;

a semiconductor layer formed on the buried oxide layer;

a first element formed in the semiconductor layer;

an epitaxial layer formed on the second region of the supporting substrate, an interface between the supporting substrate and the epitaxial layer being located at a deeper position than the position of the surface of the ~~second~~ first region;

a second element formed in the epitaxial layer, the second element including a memory cell of a DRAM, the memory cell including a cell transistor and a trench capacitor, and the trench capacitor being formed across the interface between the supporting substrate and the epitaxial layer; and

a first element isolation region interposed between the epitaxial layer and the semiconductor layer, the first element isolation region extending from an upper surface of the semiconductor layer to a position deep into the semiconductor layer, at least to an upper surface of the buried oxide layer, and the buried oxide layer and the first element isolation region jointly serving to electrically insulate the semiconductor layer from the epitaxial layer and the supporting substrate.

Claim 28 (Previously Presented): The semiconductor device according to claim 27, wherein an upper surface of the epitaxial layer is flush with the upper surface of the semiconductor layer.

Claim 29 (Previously Presented) The semiconductor device according to claim 27, wherein the supporting substrate, the semiconductor layer and the epitaxial layer are formed of silicon and the buried oxide film is formed of silicon oxide.

Claim 30 (Previously Presented): The semiconductor device according to claim 27, further comprising:

a first well region formed in the epitaxial layer, wherein a collar oxide film of the trench capacitor is formed in the first well region.

Claim 31 (Previously Presented): The semiconductor device according to claim 30, further comprising:

a second region formed in the first well region, wherein source regions and drain regions of a buried strap and the cell transistor are formed in the second well region.

Claim 32 (Previously Presented): The semiconductor device according to claim 31, wherein the buried strap electrically connects the trench capacitor and the drain region of the cell transistor.

Claim 33 (Previously Presented): The semiconductor device according to claim 31, further comprising:

a source electrode in contact with the source region and embedded in the second well region; and

a second element isolation region embedded in the second well region of the drain region.

Claim 34 (Previously Presented): The semiconductor device according to claim 27, wherein the first element includes a MOSFET which configures at least a part of a logic circuit.